

A Solid-State Driven Power Amplifier Design for the Booster RF Cavities

T. Berenc, J. Reid

8/2/2001

Abstract: *The design of a solid-state driven (SSD) power amplifier system for the Booster RF cavities is presented here along with measurements of a prototype of this design which has been installed in Booster Station 12. Details associated with the Station 12 installation are also documented.*

Introduction.....	2
The Design Model.....	2
Power Tube Operating Curves.....	4
The Cathode Circuit Design	10
CW Measurements at the RF Test Station	16
Booster Station 12 Installation.....	18
Booster Station 12 Remote Monitoring & Controls	23
Some SSD System Component Characterizations.....	24
Conclusion	26

Introduction

A solid state driven (SSD) power amplifier (PA) design for the Booster RF cavities is desired for a number of reasons; some of which include the desire to eliminate the use of the Eimac 4CW800F tubes and the desire to minimize the number of components installed in the tunnel. A SSD approach has been operating successfully in the Main Injector (MI) and thus a similar system is an attractive upgrade for the Booster. In fact, the Booster SSD design is conceptually identical to the MI system. The main technical difference between the designs is in the final tube cathode circuit where the bandwidth of the Booster is achieved.

The Design Model

A very simplified circuit topology that was used for the design is shown in Fig. 1.

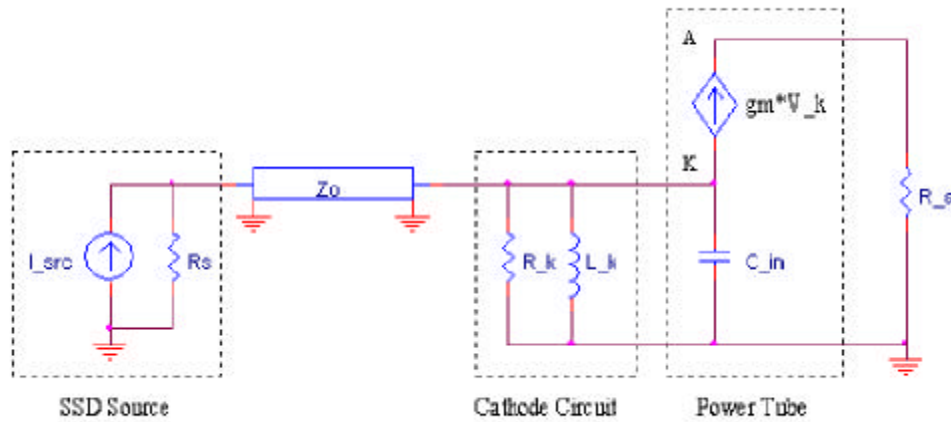


Figure 1. Very Simplified Circuit Topology of the SSD PA Design

This circuit represents the SSD source with source impedance R_s driving the cathode of a RF grounded-grid power tube through a length of transmission line of characteristic impedance Z_o . The cathode circuit, represented by R_k and L_k , is realized by a resistively loaded inductive stub which is designed to resonate with the input capacitance of the tube, C_{IN} , and to provide sufficient loading for realizing the required bandwidth of the system. The voltage-controlled-current source (VCIS) is a simplified model of the power tube response and represents the load presented to the cathode circuit due to the total cathode current in the tube. Neglecting the grid and screen currents, it is assumed that the anode current is approximately equal to this cathode current. Thus the anode and the impedance presented to the anode by the cavity at resonance, R_A , are included in the circuit for discussing the relationship between drive power and cavity power. The reactance of the cavity impedance has been neglected based upon the assumptions that the cavity is dynamically tuned to present a real impedance to the anode at the drive

frequency and that the amplification factor is large. A large amplification factor implies that the anode voltage negligibly affects the cathode current, thus it also implies a negligible influence on the input circuit by a reactive load presented to the anode either by a mistuned cavity and/or by a beam-loaded cavity.

The above assumptions are realized to be quite liberal when one knows that the cathode current of an ideal tetrode is represented by the nonlinear expression ¹,

$$I_K = b \left(V_{GK} + \frac{V_{SK}}{m_s} + \frac{V_{AK}}{m_A} \right)^{3/2}, \quad (1)$$

where β is a constant determined by the tube dimensions, V_{GK} is the grid-to-cathode potential, V_{SK} is the screen-to-cathode potential, V_{AK} is the anode-to-cathode potential, and m_s and m_A are respectively the screen and anode amplification factors. Thus, the tube actually presents a nonlinear load to the tuned cathode circuit.

However, this nonlinear load may effectively be a linear load under certain conditions; one of which is when it is a load on a high quality factor (Q) tuned circuit. This can be reasoned by considering that the DC and harmonic components of the nonlinear load current are effectively shunted to ground since they circulate around both the nonlinear load and the low impedance that the tuned circuit presents at dc and the harmonics. Thus, the harmonic components contribute little to the potential established across the nonlinear load, thereby leaving the potential a pure sinusoid at the drive frequency. The effective linear load is simply the potential across the nonlinear load divided by the fundamental component of the nonlinear load current. This reasoning is explored in detail by Clarke and Hess².

The booster design inherently dictates a low Q cathode circuit to accommodate the large booster sweep (37.5MHz to 53.1MHz) which is close to an octave. Although a high-Q assumption is required for the previous reasoning, a first order design approach is to consider the tube as an appropriately calculated effective linear load. It is this first order approach which was used for the Booster PA design. The method used to determine the effective linear load is a standard technique used in power tube analysis and will be outlined here with details relevant to the Y567 tube used in the Booster PA.

¹ Varian Eimac Laboratory Staff, "Care and Feeding of Power Grid Tubes", Varian Eimac, 1967, Library of Congress Catalog Number 67-30070

² K.K.Clarke, D.T.Hess, "Communication Circuits: Analysis and Design", Krieger Publishing Company, 1994, Reprint of Original 1971 Edition by Addison-Wesley Publishing Company, Ltd.

Power Tube Operating Curves

For the SSD PA design, the bias power supplies and cavity remain unchanged. Thus the load line and DC quiescent point are dictated by both the load impedance that the cavity presents to the tube and the desired cavity power. Table 1 and Fig. 2 represent the impedance presented to the anode, the single-gap impedance of the cavity, and the voltage step-up ratio from the anode to the single-gap. The anode impedance data came from measurements of the impedance at the anode as measured by a vector impedance meter placed between the anode and the grounded-screen of a dummy PA shell which has an exposed Y567 tube installed. The voltage step-up ratio was calculated from single frequency test-station measurements. It was calculated by dividing the achieved gap-voltage by 1kV less than the DC anode bias voltage (which is assumed to be the anode RF voltage swing). The single-gap impedance was then calculated by multiplying the anode impedance by the square of the voltage step-up ratio.

Table 1: Booster Cavity Impedance Data

Frequency (MHz)	Anode Impedance (kW)	Single-Gap Impedance (kW)	Voltage Step-Up Ratio
37	3.2	5.3	1.3
38	3.4	5.7	1.3
39	3.6	7.0	1.4
40	3.9	7.6	1.4
41	4.2	8.2	1.4
42	4.6	9.0	1.4
43	5.0	9.7	1.4
44	5.4	10.6	1.4
45	5.7	11.2	1.4
46	5.0	9.7	1.4
47	6.9	13.5	1.4
48	7.6	14.8	1.4
49	8.3	16.3	1.4
50	9.2	17.9	1.4
51	9.7	19.0	1.4
52	10.7	24.1	1.5
53	11.5	25.8	1.5

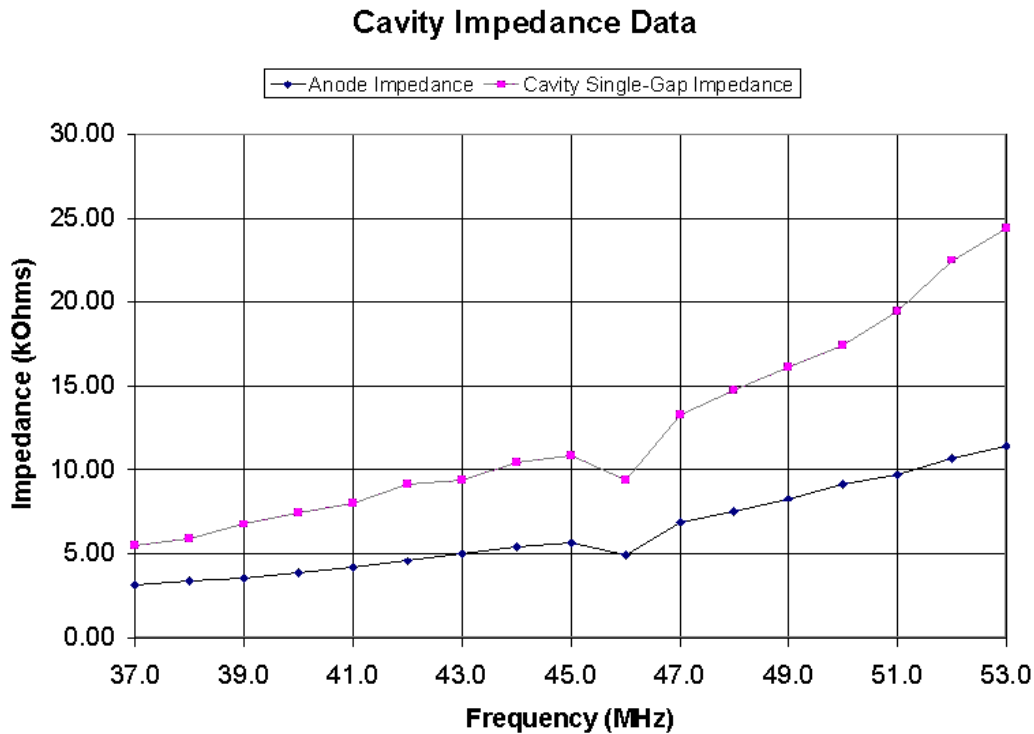


Figure 2: Cavity Impedance Data. Note: The dip at 46 MHz is real and was confirmed by further measurements and by finer frequency resolution measurements.

To obtain the tube operating curves, one uses the constant current curves for the tube. Figure 3 shows the constant current curves for a grounded grid Eimac 4CW100000E (Y567) along with an overlaid load line which will be explained shortly. The curves were obtained by using the grounded grid constant current curves supplied by Eimac and then extrapolating these curves out to include anode-to-grid voltages up to 50 KV. The tubes in the Booster have always operated past the recommended limits on the anode voltage. This is due to the low anode-to-gap step up ratio and the desired cavity gap voltage.

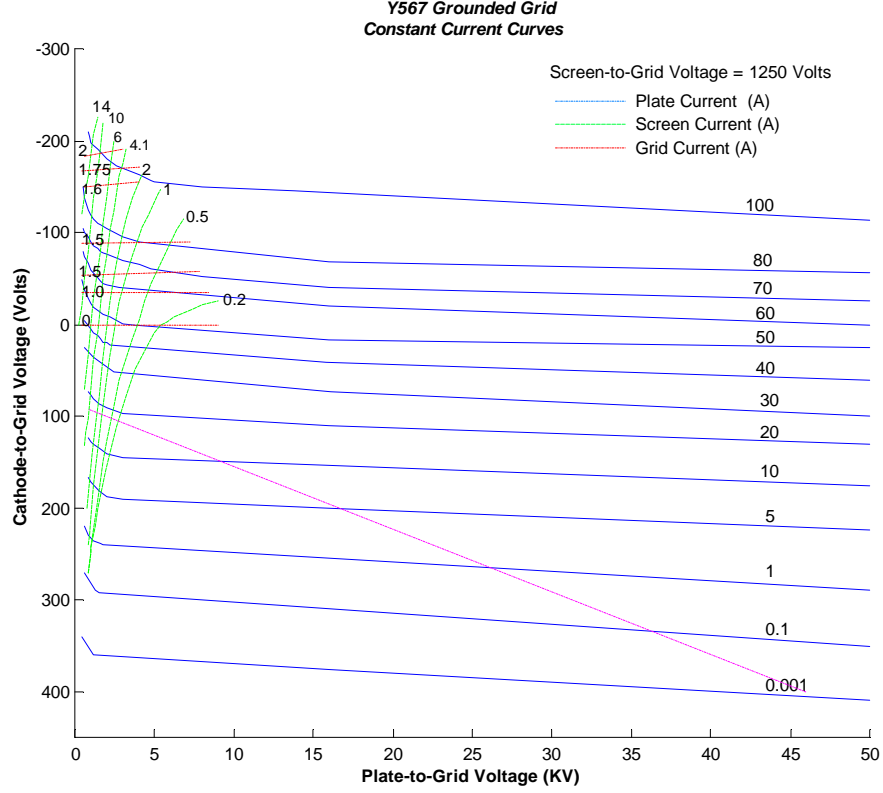


Figure 3: Y567 Grounded Grid Constant Current Curves with Typical Load Line

The load line is determined by a number of factors. First the DC bias point is chosen. The anode bias (plate-to-grid voltage) is chosen to support the required peak RF anode voltage. In the Booster the anode is typically biased around 24 KV. The peak RF anode swing is around 23 KV before screen conduction occurs since the screen is typically biased at about 1.025 KV. The achievable cavity single-gap peak voltage is thus 23 KV times the step-up ratio at the appropriate frequency. The RF anode voltage swing has to be developed across the impedance which the cavity presents to the anode (as given in Table I). Under these constraints, the only free design parameter is the cathode-to-grid bias. The bias is actually applied to the grid with the grid sufficiently bypassed at RF frequencies such that the tube can be considered RF grounded-grid.

The choice of the cathode-to-grid bias is determined based upon a trade off between required drive power and anode efficiency. This can be seen by exploring the simplest case of a small signal class A amplifier by expanding Eq. 1 into a Taylor series about the bias point. This expansion is given as

$$I_K \cong b \cdot V_{Bias}^{3/2} + \frac{3}{2} b \cdot V_{Bias}^{1/2} \cdot v_{RF} \sin(wt) + \frac{3}{8} b \cdot V_{Bias}^{-1/2} \cdot v_{RF}^2 \sin^2(wt) - \frac{3}{48} b \cdot V_{Bias}^{-3/2} \cdot v_{RF}^3 \sin^3(wt) + \dots$$

where $V_{Bias} = \left(V_{GK_{DC}} + \frac{V_{SK_{DC}}}{m_s} + \frac{V_{AK_{DC}}}{m_a} \right)$, v_{RF} is the RF cathode-to-grid drive voltage, and in which we have assumed both that the screen is sufficiently bypassed such that the screen voltage doesn't change during dynamic operation and that the anode amplification factor is large enough that the dynamic changes in V_{AK} can be neglected.

If we consider only the first two terms, we see that the cathode current consists of a DC term and an AC term. From these two terms we can gain a first order understanding of how the drive power and efficiency are effected by the choice of cathode-to-grid bias. Assuming the anode current equals the cathode current, then

$$I_A \cong b \cdot V_{Bias}^{3/2} + \frac{3}{2} b \cdot V_{Bias}^{1/2} \cdot v_{RF} \sin(\omega t) = I_{DC} + I_{ac}$$

If V_{Bias} is changed from $V_{Bias 1}$ to $V_{Bias 2}$ while still requiring the same output power (the same I_{ac}), then the cathode drive power, $P_{Drive} = \frac{1}{2} v_{RF} I_{ac}$, will change by the following ratio,

$$\frac{P_{Drive 2}}{P_{Drive 1}} = \sqrt{\frac{V_{Bias 1}}{V_{Bias 2}}}.$$

The anode efficiency, which is $h = \frac{P_{RF Out}}{P_{DC In}} = \frac{1/2 \cdot I_{ac}^2 \cdot R_a}{V_{A_{DC}} I_{DC}}$, will change by the following ratio,

$$\frac{h_2}{h_1} = \left(\frac{V_{Bias 1}}{V_{Bias 2}} \right)^{3/2}.$$

Thus, it is clear that if the cathode-to-grid bias is raised, the drive power requirement is decreased, but so is the tube's efficiency.

Traditionally, the booster and MI final tubes have operated in class AB with the grid biased around $-300V$. This choice of bias was a starting point for the design and allowed for calculating reasonable tube transconductance values which influence the cathode circuit design.

The constant current curves in Fig. 3 were used to determine a load line which had the following properties: 1.) a proper DC bias point, 2.) screen conduction, and 3.) a required RF load on the anode equal to the impedance which the cavity presents to the anode. The screen conduction stipulation is due to the fact that amplitude regulation is achieved by requiring the screen to conduct. The RF load on the anode varies with operating frequency as Table 1 has shown. Thus various load lines were simulated.

Another subtle, but crucial, point about these simulations was that the constant current curves had to be scaled appropriately to take into account the actual screen voltage used. This scaling is quite simple and can be done using Eq. 1. For a detailed discussion of this scaling see pages 97 and 98 of “Care and Feeding of Power Grid Tubes” by Varian³.

Results of various tube load line simulations using a code written in Matlab are shown in Table 2. The code was written to allow a user to graphically choose a DC bias point and the load line end point directly on the constant current curves along with specifying the phase angle between cathode and anode to allow for reactive loads. The instantaneous grid, screen, and plate currents are then interpolated from the curves. The code then calculates a DC component, the fundamental component, and a user-defined number of harmonic components of these currents. The DC component is used to determine the power supply requirements. The fundamental component of the anode current is used in conjunction with the RF anode voltage swing to determine the required anode load which would result in this load line. The code assumes a pure sinusoidal cathode-drive voltage, a pure sinusoidal anode voltage swing on the load, a perfectly bypassed screen, and an ideal tube with no interelectrode feedback capacitances.

³ Varian Eimac Laboratory Staff, “Care and Feeding of Power Grid Tubes”, Varian Eimac, 1967, Library of Congress Catalog Number 67-30070

Table 2: Results of Tube Operating Simulations for two different Grid Bias and Anode Impedance conditions.

	~3kOhm Load Line @-300V Grid Bias	~11.5kOhm Load Line @ 300V Grid Bias	~3kOhm Load Line @-250V Grid Bias	~11.5kOhm Load Line @-250V Grid Bias
Cathode-to-Grid Bias Voltage (V)	300	300	250	250
Grid Bias Current (A)	0	0	0	0
Screen-to-Grid Bias Voltage (V)	1300	1300	1250	1250
Screen Bias Current (A)	0	0	0	0
Plate-to-Grid Bias Voltage (kV)	23.9	24.1	24	24.2
Plate Bias Current (A)	0.6	0.6	1.9	1.8
Peak RF Cathode Drive Voltage (V)	187.8	95.7	144.6	61.0
Peak RF Plate-Voltage (kV)	22.6	23.1	22.9	23.3
DC Plate Current (A)	4.5	1.4	5.2	2.2
RF Plate Current @fo (A_peak)	7.3	1.9	7.7	2.0
RF Plate Current @2fo (A_peak)	3.9	0.8	3.1	0.3
RF Plate Current @3fo (A_peak)	1.0	0.1	0.3	0.3
Peak Plate Current (A)	15.9	4.1	15.8	4.6
Power From Plate Bias Supply (kW)	107.2	32.5	123.3	53.9
Tube Transconductance (A/V)	0.04	0.02	0.05	0.03
Available RF Power (kW)	83	22.5	88.3	23.5
Tube Plate Dissipation (kW)	24.2	10.0	35.1	30.5
Plate Efficiency (%)	77.4	69.2	71.6	43.5
Required RF Load (Ohm)	3086	11873	2959	11580
DC Screen Current (A)	0.14	0.06	0.18	0.09
RF Screen Current @fo (A_peak)	0.27	0.12	0.35	0.17
RF Screen Current @2fo (A_peak)	0.26	0.12	0.34	0.17
RF Screen Current @3fo (A_peak)	0.25	0.011	0.32	0.16
Peak Screen Current (A)	2.24	1.32	2.88	1.76
Power From Screen Bias Supply (W)	177.3	77.4	223.7	108.8
DC Grid Current	0	0	0	0
RF Grid Current @fo (A_peak)	0	0	0	0
RF Grid Current @2fo (A_peak)	0	0	0	0
RF Grid Current @3fo (A_peak)	0	0	0	0
Peak Grid Current (A)	0	0	0	0
Power Absorbed by Grid Supply (W)	0	0	0	0

As discussed previously, for a fixed anode impedance, Table 2 shows that the transconductance increases and the efficiency decreases as the tube is turned on harder with a lower cathode-to-grid bias. Also note how the efficiency decreases as the anode impedance increases. The transconductance is found by dividing the fundamental RF anode current by the cathode drive voltage. The inverse of the transconductance is the effective linear load that the tube presents to the cathode circuit. Notice that the transconductance decreases as the anode impedance is raised.

The Cathode Circuit Design

Since the required gap voltage is nearly constant across the Booster frequency sweep, the power levels needed are highest for the lowest anode impedance, which occurs at the lowest frequency of 37 MHz. This also means that the drive power requirements are highest here also. Thus, the cathode circuit is designed to be matched closer to the low frequency extreme while still maintaining a reasonable response at the high frequency extreme. The value of transconductance that was used for the design was 0.035 A/V which was a compromise between the drive power requirements, the frequency response, and the physically realizable values of the RF components used in the design. The details of the cathode circuit design are now discussed.

Replacing the voltage-controlled current source of Fig. 1 with a single resistive load equal to the inverse of the transconductance of the tube, the cathode circuit model becomes that shown in Fig. 4.

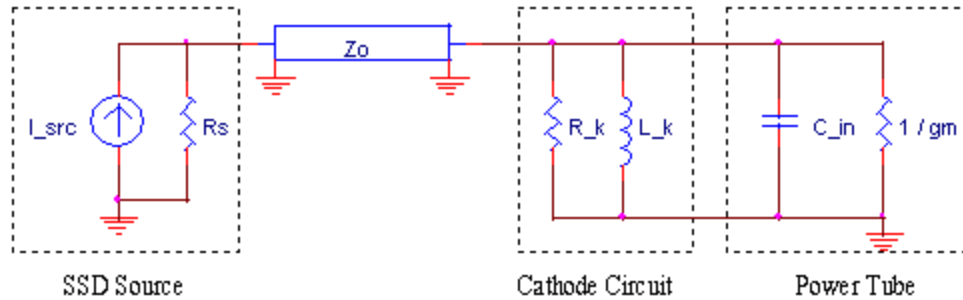


Figure 4: Reduced Cathode Circuit Model with tube transconductance loading

The transconductance design value was chosen to be 0.035 A/V, the inverse of which is 28.6 Ohms. The input capacitance of the tube, C_{IN} is approximately 250 pF. This includes the tube socket configuration. The values of L_K , R_K , Z_0 , and R_S are chosen to achieve a desired frequency response. For matching considerations the source impedance, R_S , and the characteristic impedance of the interconnecting transmission line, Z_0 , are chosen to be equal.

The cathode circuit design equations are dictated by the equations for a simple RLC resonator driven by a source of impedance Z_o . The design equations which can be derived from various forms found in standard literature are:

$$f_o = \sqrt{f_1 f_2}$$

$$Q_L = \sqrt{10^{a/10} - 1}$$

$$L_K = \frac{1}{(2\pi f_o)^2 C_{IN}}$$

$$R_{Total} = \frac{Q_L}{2\pi f_o C_{IN}}$$

$$R_{Total} = R_K // \frac{1}{g_m} // Z_o = \frac{Z_o R_K}{Z_o (1 + g_m R_K) + R_K}$$

$$Z_{IN} = R_K // \frac{1}{g_m} = \frac{R_K}{1 + g_m R_K}$$

where f_o is the resonant frequency, which is the geometric mean of f_1 and f_2 , the lower and higher frequency extremes respectively at which the magnitude response is attenuated by α dB from the response at f_o . Q_L is the loaded quality factor of the circuit. R_{Total} is the total resistive load on the resonant circuit and consists of the parallel combination of R_K , $1/g_m$, and Z_o . Z_{IN} is the resonant impedance presented to the transmission line by the cathode circuit.

The ideal situation is to have Z_{IN} equal to Z_o at resonance, thereby matching the transmission line and reducing the drive power requirements due to losses in reflected energy. If Z_{IN} is to equal Z_o at resonance, then R_K is given as

$$R_K = \frac{Z_o}{1 - g_m Z_o}.$$

Values of Z_o which are easily attainable are parallel combinations of 50 Ohms. Values which were investigated were 50 Ω , 25 Ω , and 12.5 Ω . Z_o was chosen as 12.5 Ω due to a number of reasons. The available power combiner for the SSD amplifiers had an output impedance of 12.5 Ω . Also, this value for Z_o , in combination with a nominal value of 0.035 A/V for g_m , resulted in R_K equaling 22.2 Ω , which is closely realized with two 50 Ω loads in parallel. And finally, this value provides a reasonable magnitude and phase response for the cathode circuit.

Results of cathode circuit simulations using $Z_0 = 12.5\Omega$, $R_K = 22.2\Omega$, $f_1=37\text{MHz}$, $f_2=54\text{MHz}$, $C_{IN} = 250\text{pF}$, and $L_K = 50.7\text{nH}$ are shown in Fig. 5. These are only approximations since in actuality $R_K = 25\Omega$ and L_K is realized using a resistively loaded inductive shorted-stub transmission line. The simulations were performed using three values of g_m . The anode impedance values used to calculate required power levels were those given previously in Table 1. Although the simulations are approximations, the information is useful for determining trends and expected power requirements.

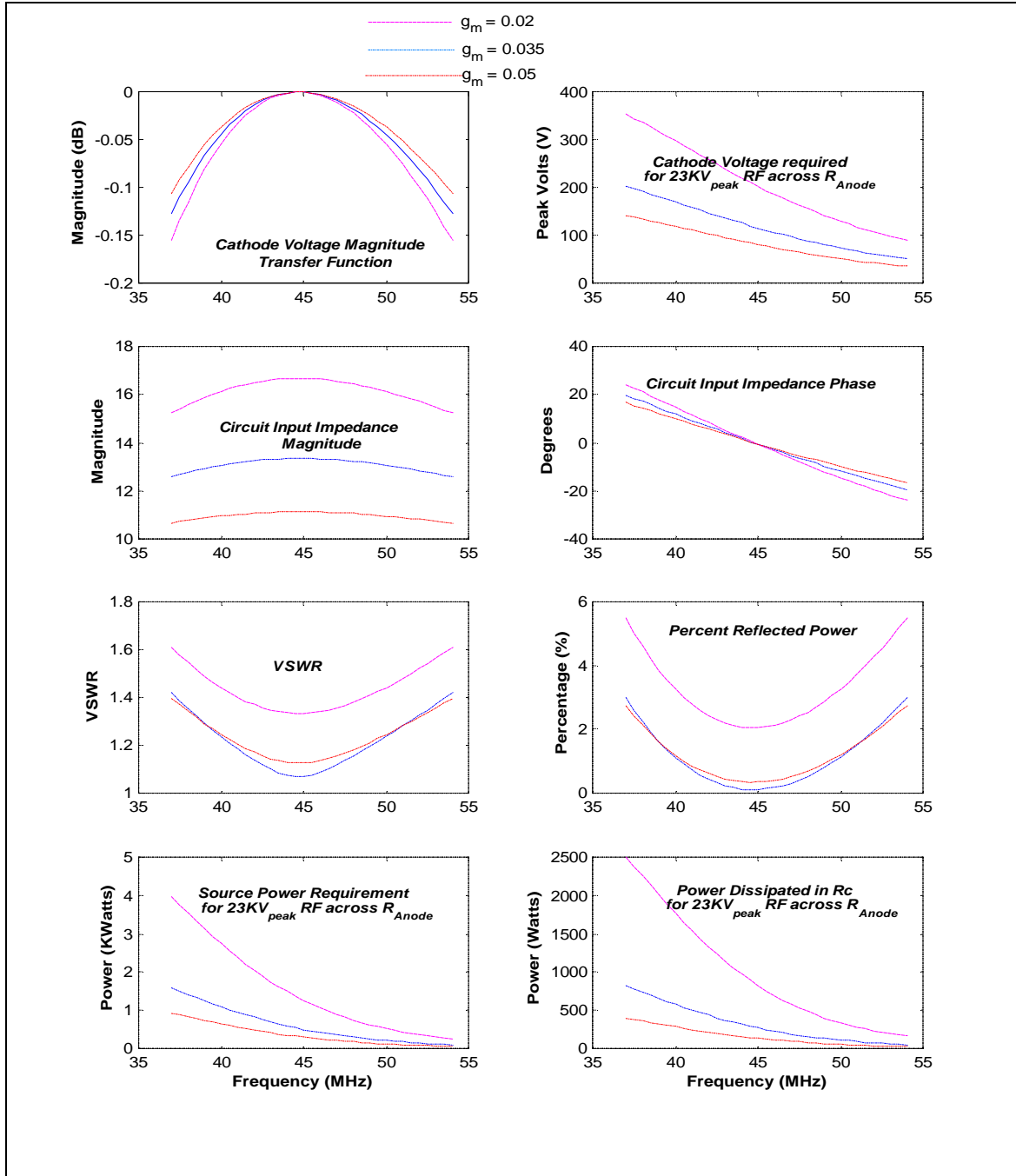


Figure 5: Cathode Circuit Simulation Results

A cross sectional view of the PA is shown in Fig. 6. The bottom half consisting of the grid, screen, and anode assemblies is an exact copy of the MI PA. The top half is the cathode circuit. It consists of an inductive shorted stub which accommodates the RF drive connections, the cathode load connection, the filament heater voltage leads, and water cooling. The RF drive connections and the cathode load connection are located right at the cathode. The overall length of the inductive stub had to achieve the required inductance and had to allow the PA to fit in the Booster tunnel. This was achieved by tapering the inner conductor of the stub to realize a higher characteristic impedance than the stub used in the MI design; thereby achieving the desired inductance value within the height constraints of the tunnel.

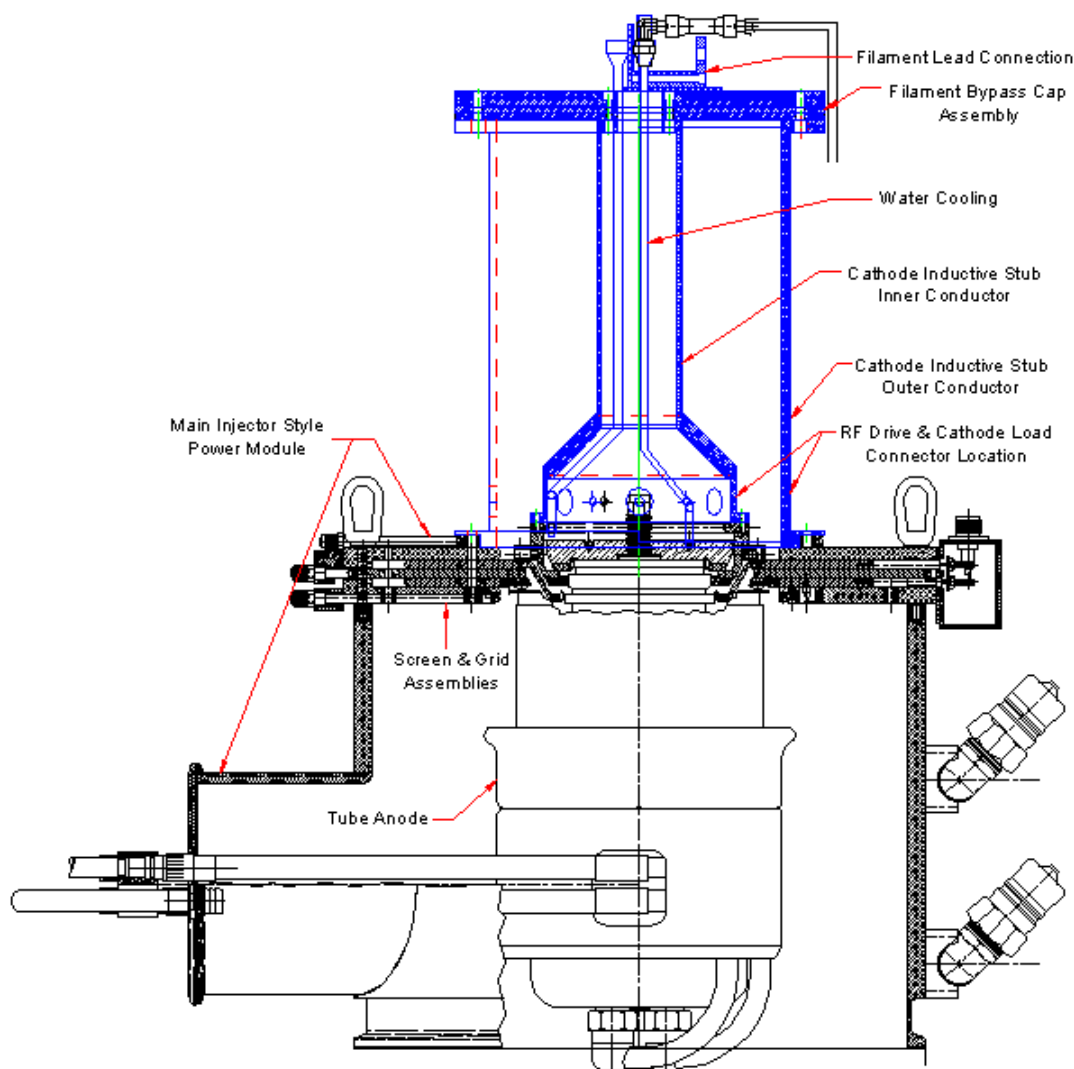


Figure 6: Prototype SSD PA Cross Sectional View

A circuit schematic of the PA, excluding stray reactances and losses, is shown in Fig. 7. The schematic is filed as drawing number 0333-EC-181896.

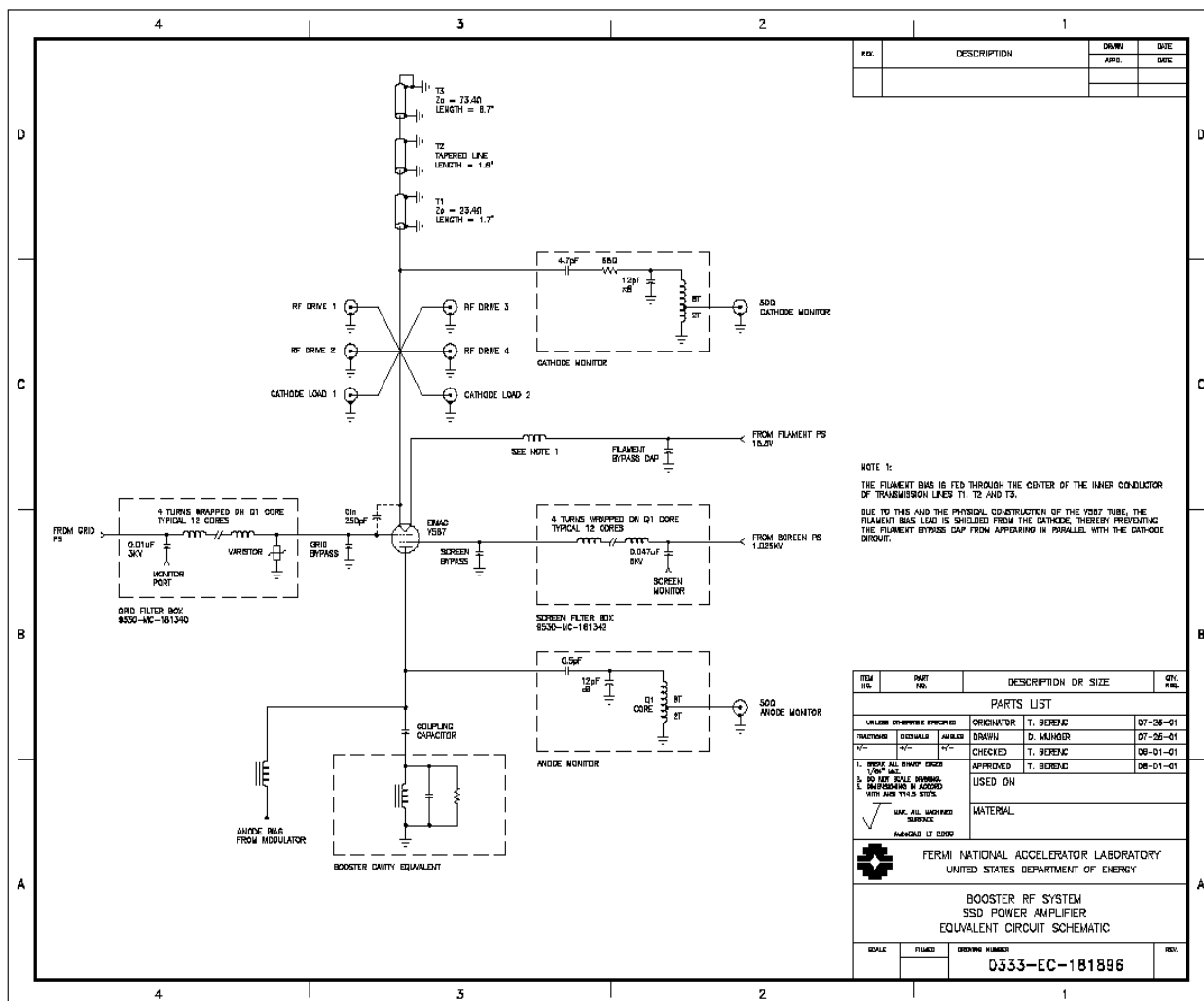


Figure 7: PA schematic, drawing #0333-EC-181896

A list of the drawing numbers associated with the cathode circuit is given in Table 3.

Table 3: List of mechanical drawings associated with the SSD PA Cathode Circuit

Drawing Number	Description
0333-MD-181767	Cathode Resonator Inner Conductor
0333-MD-181768	Cathode Resonator Outer Conductor
0333-MD-181769	Filament Bypass Capacitor Bottom Plate
0333-MD-181770	Filament Bypass Capacitor Top Plate
0333-MD-181771	Filament Bypass Capacitor Electrode
0333-MD-181772	Filament Bypass Capacitor Dielectric
0333-MD-181773	Filament Lead Connection Clamp
0333-MD-181774	Filament Lead Clamp Isolation Plate
0333-MD-181775	Filament/Cathode Insulator
0333-MD-181776	Filament Bypass Capacitor Electrode Connection Backing-Plate
0333-MB-181895	Cathode Monitor Mounting Plate

Figure 8 shows a measurement of the cathode assembly without tube transconductance loading. The measurement was taken by terminating all of the 'RF Drive' ports of Fig. 7 with 50Ω loads and placing a network analyzer between the 'Cathode Load' ports. The filament was heated and the grid was biased at -350V for the measurement. The cathode-to-grid capacitance with a hot filament is different from that with a cold filament. This is due to thermal expansion of the tube's internal geometry.



Figure 8: Cathode Assembly Response Measurement without tube transconductance loading, with a Hot Filament and Grid Bias=-350V

More importantly, Fig. 9 shows the cathode circuit response within a typical system installation. This response includes an Intech Solid-State Amplifier, a power combiner and four 52 feet, 50Ω cables between the power combiner and the cathode circuit. The tube loading was simulated by placing another 50Ω load in parallel to each cathode load. The network analyzer was placed between the Intech input and one of the cathode loads. The ripples in the response are due to the multiple mismatch occurring between the power combiner output and the cathode circuit input. The response looks more flat at the booster frequency extreme. However, investigations showed that the response was artificially shifted upwards due to reactance of the loads that were used to simulate the tube loading. The absolute magnitude of the response measurement is to be disregarded, it involved various attenuators and other gain elements. What is of importance is the flatness of the response.

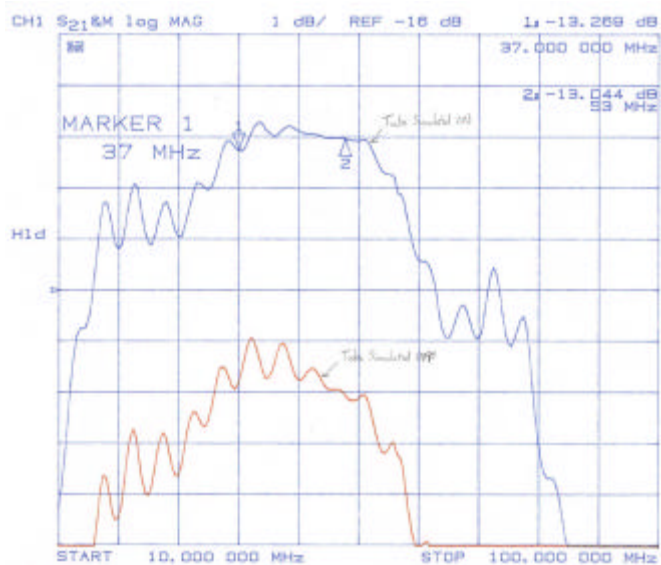


Figure 9: Cathode Circuit Response in a typical system setup with a hot Filament and biased Grid. The red trace is without simulated tube loading. The blue trace is with simulated tube loading.

CW Measurements at the RF Test Station

The prototype SSD PA was mounted onto a standard Booster cavity at the MI-60 RF Test Station for CW measurements. The test station setup mimics a typical SSD PA system like that of the MI. The output of four SSD Intech amplifiers are combined through a power combiner which has four 50Ω inputs and whose output consists of four parallel 50Ω outputs, resulting in a 12.5Ω output. The cavity was tuned to a fixed frequency by fixing the Ferrite Bias Power Supply to a static level. The tuning was initially adjusted until a maximum cavity-gap level was achieved for a fixed RF drive level. Then the tuning was optimized by adjusting for maximum screen current at a fixed drive level. A picture of the prototype SSD PA at the test station is shown in Fig. 10.

Results of the CW measurements are shown in Fig. 11. All measurements were taken with an Anode bias of 18 KV, a Grid bias of -250 V, and an achieved screen current of 300 mA. The anomaly seen at 46MHz is real as explained previously in the section “Power Tube Operating Curves” in which the cavity impedance data was presented in Table 1 and Figure 2.

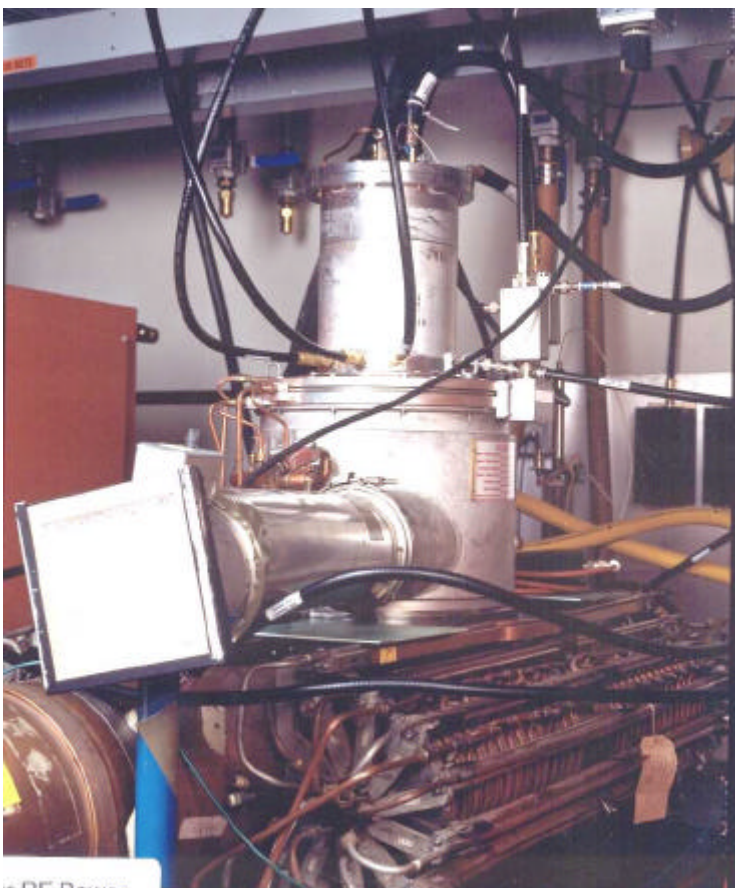
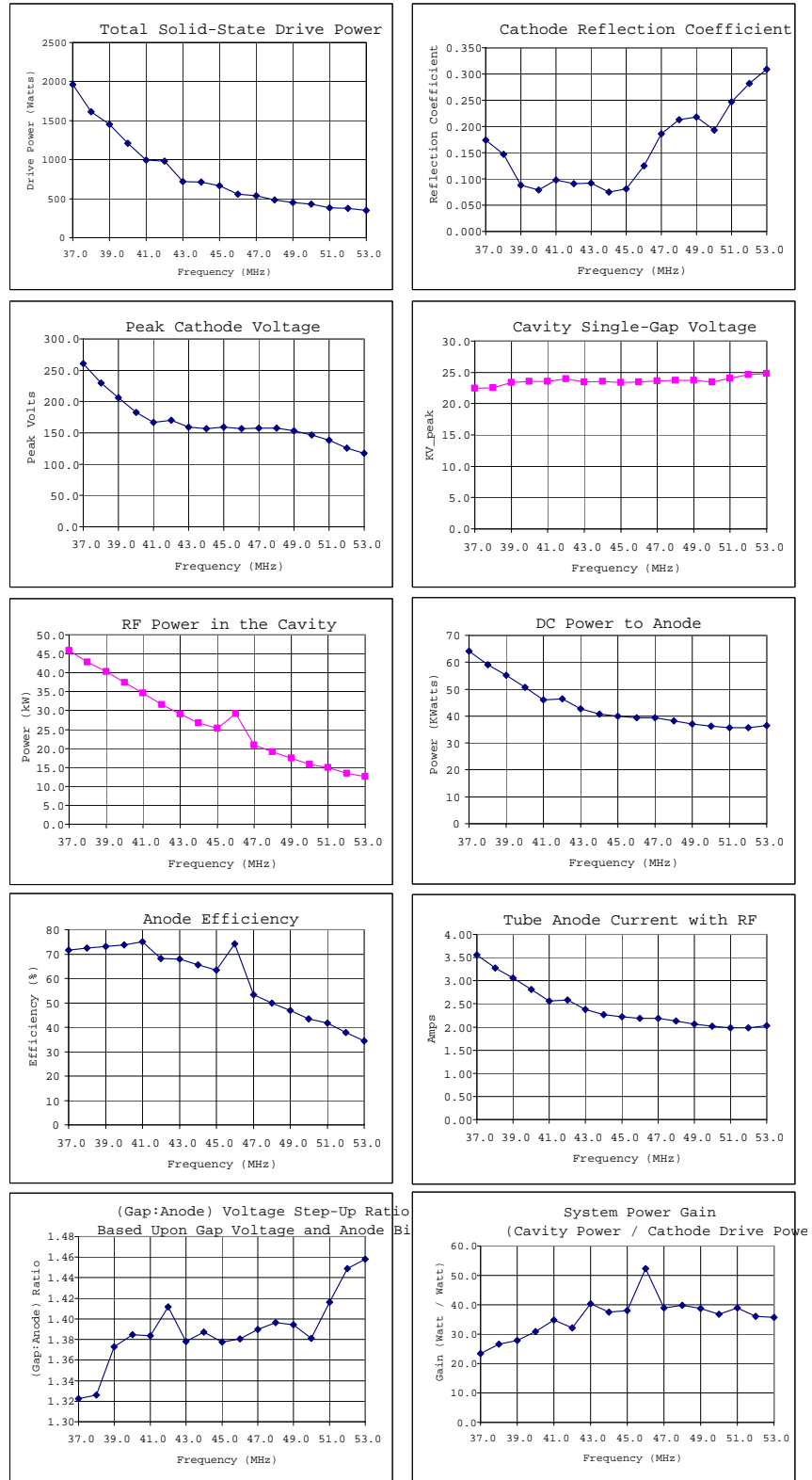


Figure 10: Prototype SSD PA mounted on a standard Booster cavity at the MI-60 RF Test Station

Figure 11: Results of CW Measurements at the RF Test Station with 18KV Anode Bias, -250V Grid Bias, and 300mA of screen current.



Booster Station 12 Installation

After the SSD PA design was thoroughly tested at the RF Test Station, it was installed into Booster Station 12 on May 5, 2001. Station 12 was chosen since its location in the RF Gallery had enough real estate for the installation of the additional SSD rack that was needed for the Intech SSD amplifiers. The installation involved replacing the Booster style Anode Modulator with the MI-style Modulator. A picture of the PA sitting on Cavity 12 in the tunnel is shown in Fig. 12. A picture of the RF Gallery at Station 12 is shown in Fig. 13.



Figure 12: Prototype SSD PA mounted on Booster Cavity 12

A block diagram of the installation is shown in Fig. 14. This block diagram is filed as drawing number 0339.000-ED-181868. Some of the existing Station 12 cables were used for the SSD system, however some new cables were installed. A cable list along with associated delay times is documented as drawing number 0339.000-ED-181898. The overall system time delay was adjusted to mimic the original system's delay. More will be said on this later.



Figure 13: Prototype SSD PA System Racks in RF Gallery at Booster Station 12

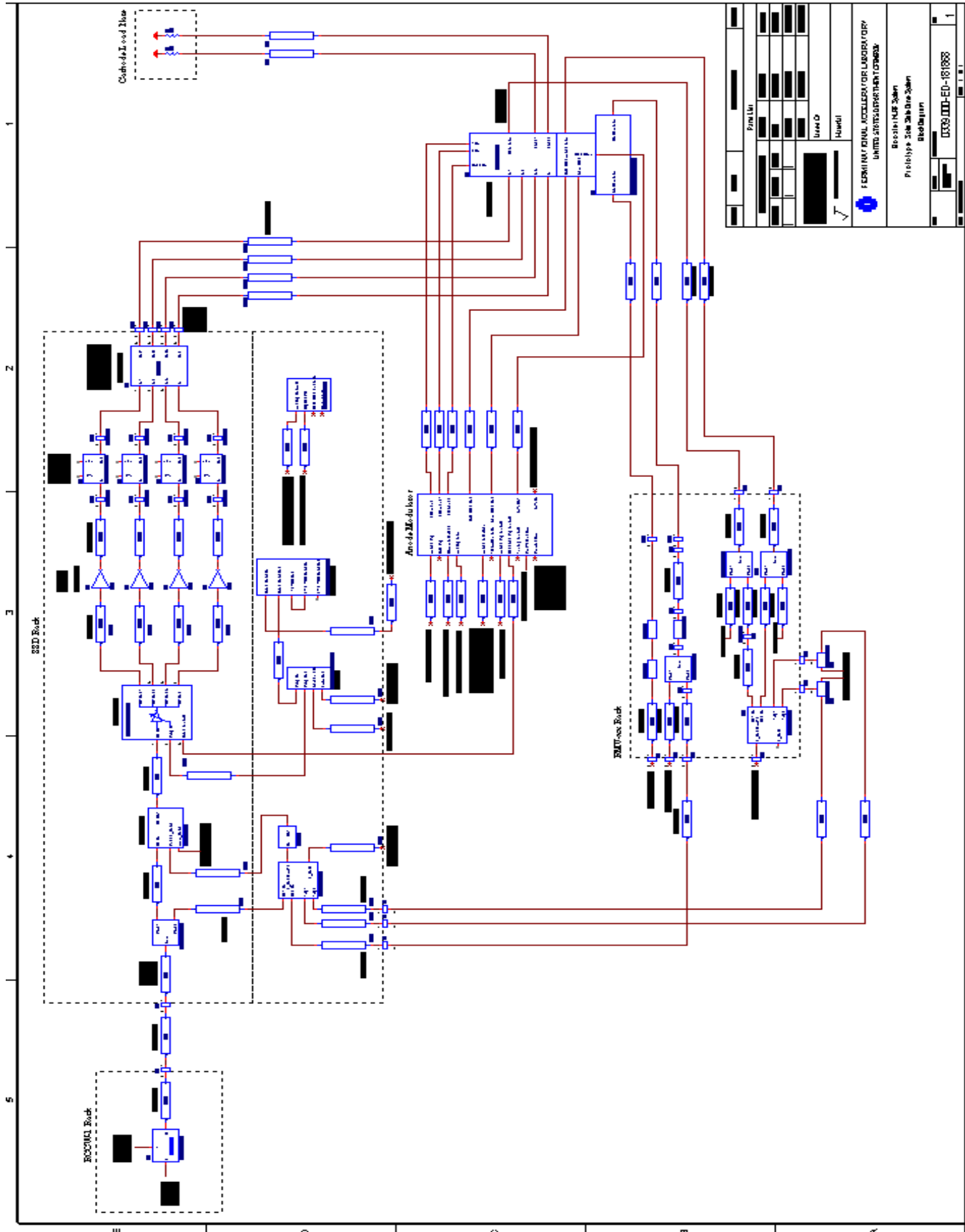
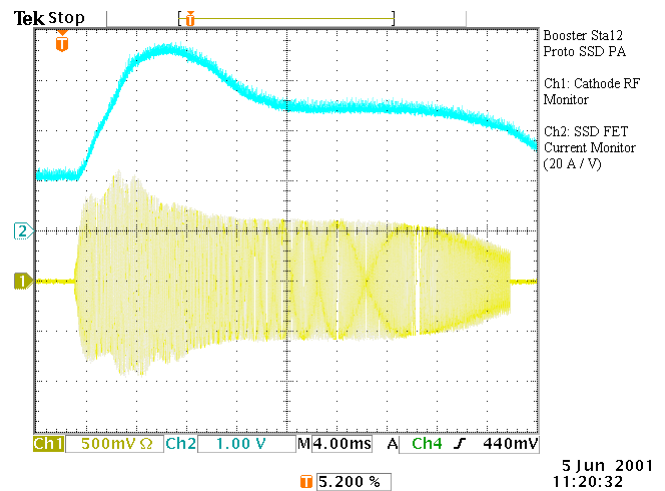
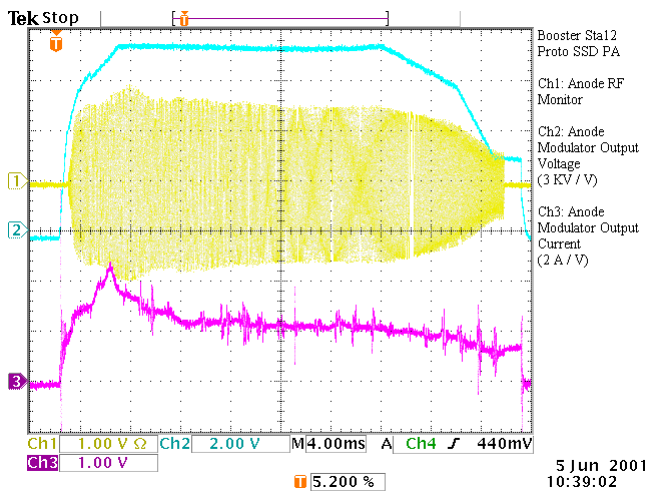
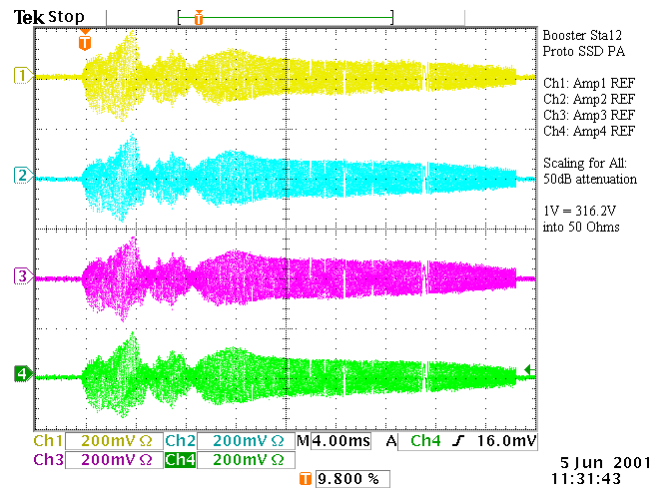
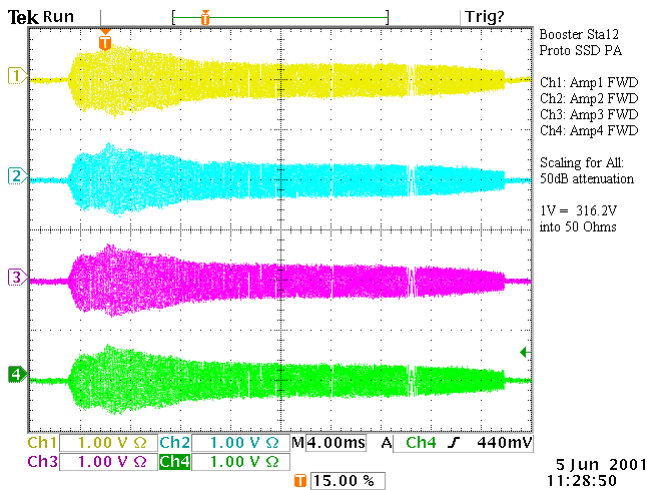
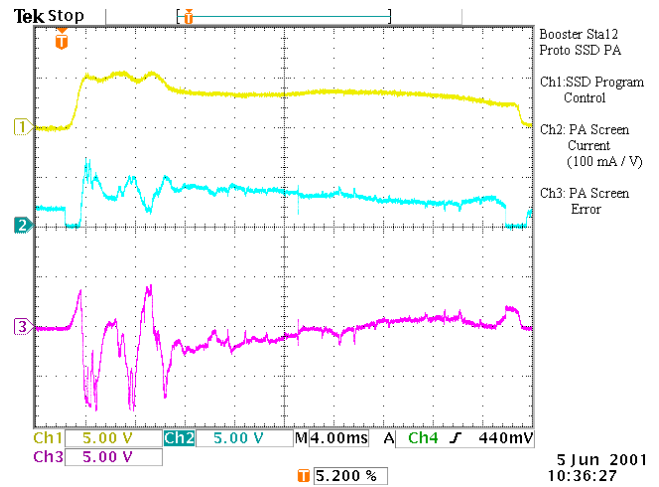
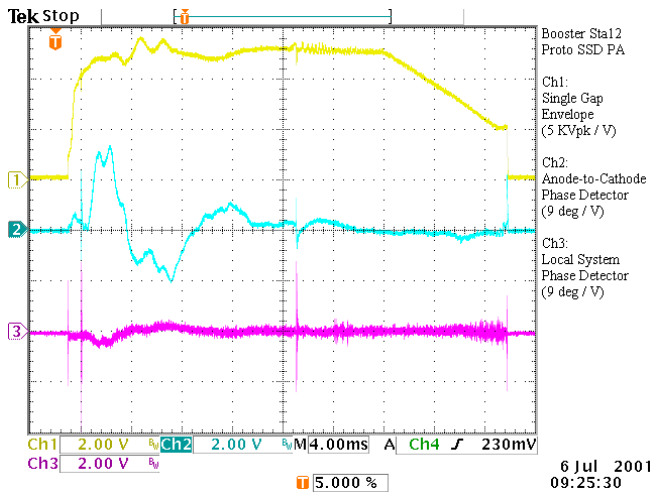


Figure 14: Prototype SSD System Block Diagram (drawing 0339.000-ED-181868)

A typical set of system operating curves for the prototype SSD system at Station 12 can be found below. These plots were taken directly at Station 12 during normal Booster operation with beam.



The overall system time delay of the prototype SSD system was matched to the original installation at Station 12 by comparing a phase measurement of Station 12 with respect to Station 16 before and after the system installation. Stations 12 and 16 are considered “sister” stations in that they are supposed to have identical time delays; therefore they should be in phase with each other throughout the Booster cycle. Cable CA2 of the block diagram was the adjustable element used for the final matching.

Figure 15 shows the comparison between the original system and the prototype SSD system. Both traces have the same scaling. The SSD system measurement closely resembles a typical local phase detector measurement of an original system. This is due to the fact that the SSD system now incorporates an overall system phase control loop as well as an Anode-to-Cathode phase detection tuning control loop as seen in the system block diagram.

This system phase control loop tries to force the overall system to look like a pure time delay. Thus measuring Station 12 with respect to 16 is like measuring Station 16 with respect to a pure time-delay cable; which is exactly the measurement that the original local system phase detectors are setup to measure and use as the error signal for the cavity tuning system. The SSD system does not adjust the cavity tuning to make up for system dispersion like the original system does.

Instead two loops are used: one for cavity tuning, and one for system dispersion. A more detailed discussion of the Booster phase control loops will be discussed in an RFI Note to follow.

However for a taste of what the two loops can achieve look at the

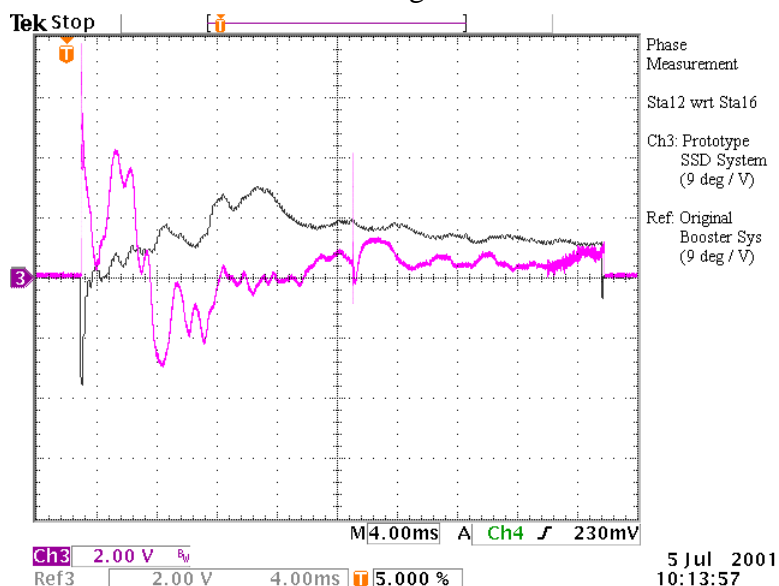


Figure 15: System Phasing Comparison - Black trace is a measurement of the original system while the Magenta trace is the prototype SSD system.

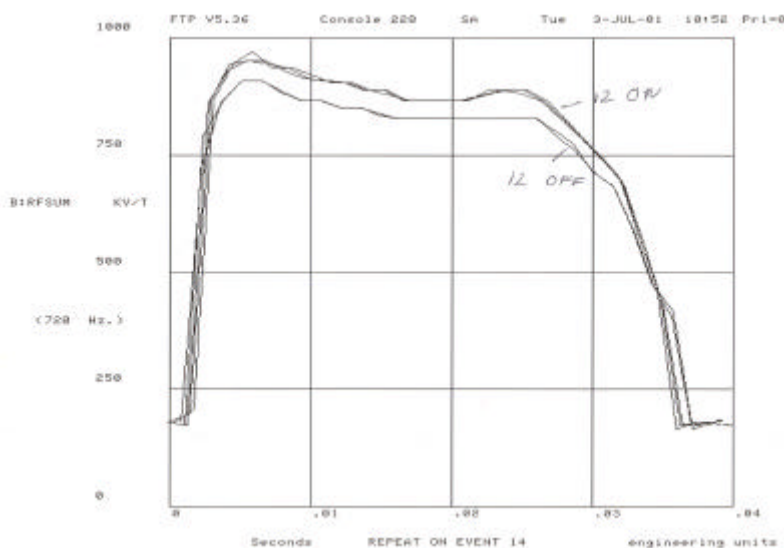


Figure 16: RF Sum Signal with and without Station 12

typical station operating curves in showing the Anode-to-Cathode phase detector and the System phase detector.

Another measurement that confirms that the SSD system's delay was properly set is a measurement of the vector sum of all the RF cavity gap voltages. If the system delay is properly set, Station 12 should add to the RF sum throughout the entire cycle. Figure 16 represents such a measurement. It depicts the RF sum signal with and without Station 12 on. As shown, Station 12 adds to the sum during the entire cycle.

Booster Station 12 Remote Monitoring & Controls

In order connect the prototype SSD system into the remote monitoring and control system, modifications had to be made to the Internet Rack Monitor, its associated interfacing unit called the Digital Cross Connect, and the parameter pages. A list of documents detailing the analog and digital status monitoring assignments is shown in Table 4.

Table 4 : List of drawings documenting remote monitoring assignments

Drawing Number	Description
0337.020-EA-181861	Digital Cross Connect (DCC) J6 & J7 Pin Assignments
0337.020-EA-181862	Digital Cross Connect (DCC) J8 & J9 Pin Assignments
0337.020-EA-181863	Digital Cross Connect (DCC) J10 & J11 Pin Assignments
0337.020-EA-181864	Digital Cross Connect (DCC) Monitor Words 0,1,2,3 Assignments
0337.020-EA-181865	Digital Cross Connect (DCC) Monitor Words 4,5,6,7 Assignments
0337.020-EA-181866	Digital Cross Connect (DCC) Control Words 0,1 Assignments
0337.020-EA-181867	Internet Rack Monitor (IRM) Analog Channel Assignments

Some very important information is a list of the scaling factors for the various monitoring points of the system. Table 5 lists the scaling factors for the signals provided at the RMU rack patch panel for Station 12.

Table 5: Scaling Factors for RMU Rack Patch Panel Monitoring Signals

Signal	Scaling
RF Gap Envelope (Single-Gap)	5 KV _{peak} / V
Anode-to-Cathode Phase Detector	9 deg / V
Local System Phase Detector	9 deg / V
Anode Modulator Voltage	3 KV / V
Anode Modulator Current	2 A / V
Ferrite Bias Supply Voltage	5 V / V
Ferrite Bias Supply Current	250 A / V
PA Grid Voltage	50 V / V
PA Screen Current	100 mA / V
SSD FET Current	20 A / V
SSD FWD Power Monitor	1V=316.2V in 50Ohms
SSD REF Power Monitor	1V=316.2V in 50Ohms

Some SSD System Component Characterizations

In order to convey information that is useful to others who may need to design with this system for purposes such as amplitude regulation, beam-loading compensation, etc., a few of the main components of the SSD system are characterized here.

The Intech amplifier magnitude response is shown in Fig. 17. This is an S_{21} 'through' response which was made by placing a network analyzer between the input and output of an Intech solid-state amplifier, with, of course, a high power 50dB attenuator on the output of the Intech amp. The attenuator was calibrated out. Thus the measurement is a true response of the Intech amplifier driving a 50 Ω load. The red trace is the response with 0dBm of drive power out of the network analyzer. With approximately

45.5dB to 47dB of gain as represented by the response, this implies that the Intech was delivering between 35.5 W and 50 W to a matched load. The blue trace represents the response with 15dBm of drive power from the network analyzer. From the response this corresponds to approximately 1kW of power from the Intech amplifier into the matched load.

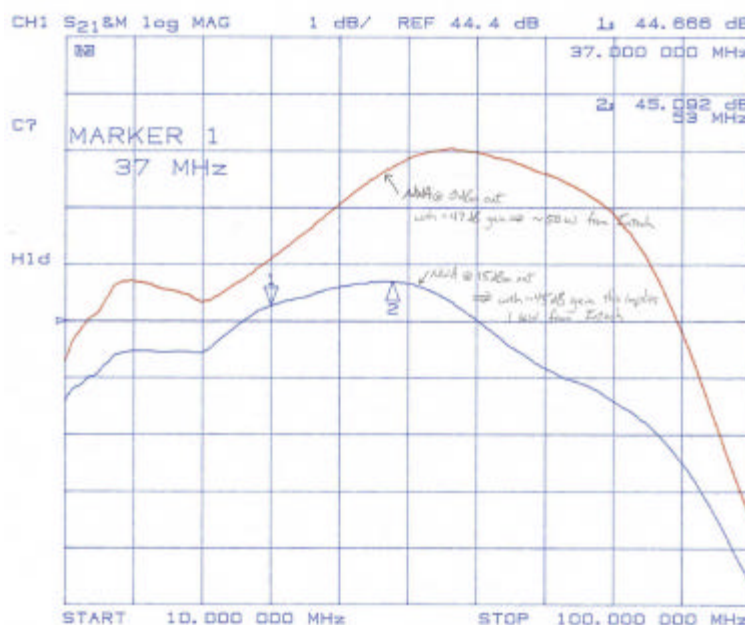


Figure 17 : Intech Solid-State Amplifier magnitude response into a matched load.

The power combiner used in the Booster SSD system is similar to the power combiner used in the MI system, which is made by Werlatone. The original combiner is fairly narrowband and was not designed to present a matched load at the center of the Booster band. Thus the quarter wave-length line inside the Wilkinson divider was increased by a factor of 1.35 to shift the match point towards the center of the Booster band. Figures 18 and 19 represent an s_{11} measurement at one of the inputs and an s_{21} measurement from one of the inputs to one of the outputs with all other ports properly terminated. The combiner is really an 8-port device and thus has a 64-element s-parameter matrix. The data for all 64 s-parameters was measured and is available on request.

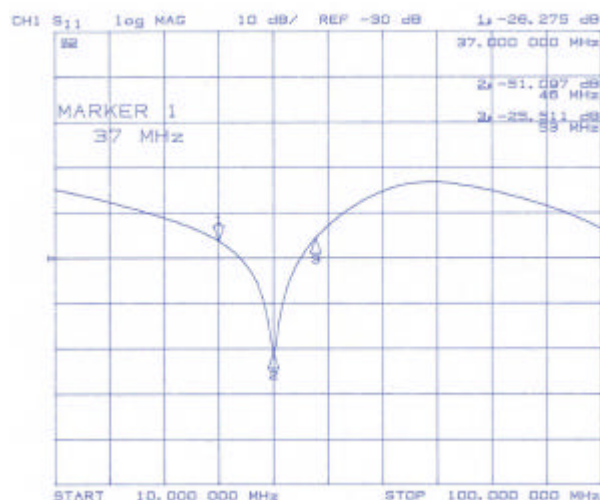


Figure 18: Modified MI-style Werlatone power combiner s_{11} measurement at one of the inputs with all other ports properly terminated.

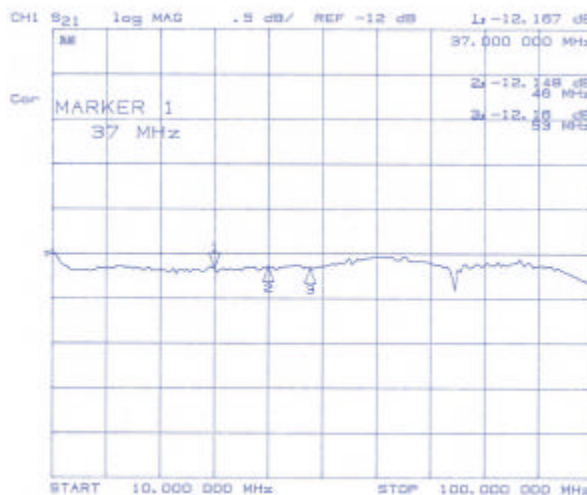


Figure 19: Modified MI-style Werlatone power combiner s_{21} measurement from one of the inputs to one of the outputs with all other ports properly terminated.

For a true characterization of the overall system, one would need to know the s-parameters for all of the devices installed into the system as a function of frequency and power levels. This data is beyond the scope of this note. A rough approximation to the overall system magnitude response which may be useful for other system designers was previously shown in Fig. 9, in which the response from the input of an Intech amp to the cathode circuit was displayed. Also, the system power gain from the total Intech amplifier output to the cavity was calculated for the CW measurements at the RF Test Station as shown in Fig. 11. This gain offers the additional information of the tube gain and cavity step-up ratio.

Conclusion

A prototype SSD PA design has been documented. This document can be used to evaluate the SSD system performance and to determine overall power requirements of both the solid-state drivers and the anode power supply. A robust system integration should involve the use of more solid-state drivers for increased drive power head room, especially if this PA will be used for a large aperture Booster cavity. Furthermore, a wider bandwidth power combiner could improve system performance.

One more thing to consider if this design is to be incorporated into the Booster is the 480V AC power distribution for the Bias Supplies and Anode Modulators. Currently, the Booster Modulators are tapped off of the Bias Supply 480V AC. During a Booster pulse, the Bias supply causes a slight imbalance in the 480V AC to the Modulators. The PA filament power supplies are sensitive to this imbalance and can sometimes see this as being an AC phase loss failure. To improve the AC power to the Modulators, separate power lines should be run directly to the Modulators.

I would like to thank everyone who helped to manifest the Booster Station 12 prototype system. Rick Zifko, Darren Plant, and Jim Hicks installed the PA, cabling, SSD Racks, and Anode Modulator. They also helped build the Booster RF Test Station. John Zuk put together the prototype PA. Lin Winterowd and Bob Goodwin programmed the remote control status pages. Jim Ranson and his team installed the required AC power for the SSD racks and Anode Modulator. Jim Lackey and Bob Webber emptied and filled the tunnel cable penetration and provided installation information. And I sincerely, sincerely apologize if I have forgotten anybody.